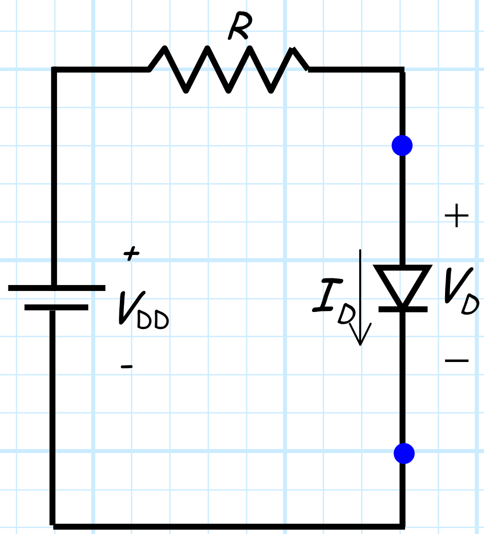
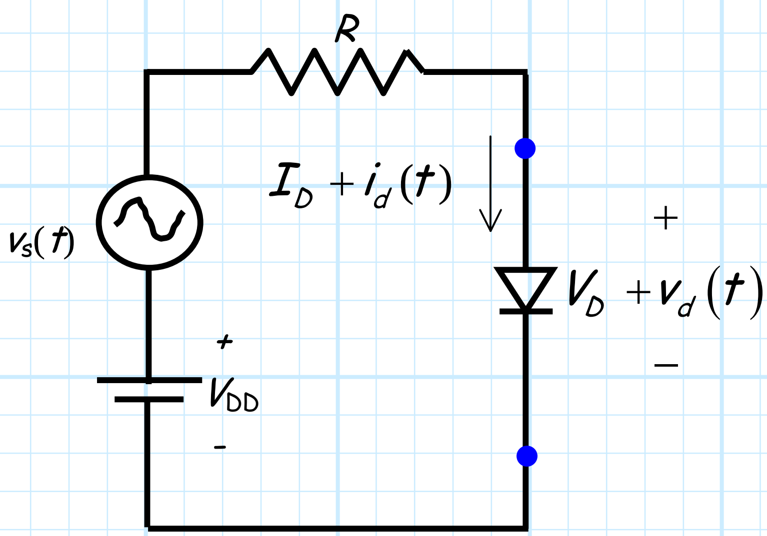
Small-Signal Analysis

Consider this simple **junction diode** circuit:



The **DC voltage source** (V_{DD}) results in a **DC current** (I_D), as well as a **DC voltage** across the junction diode V_D.

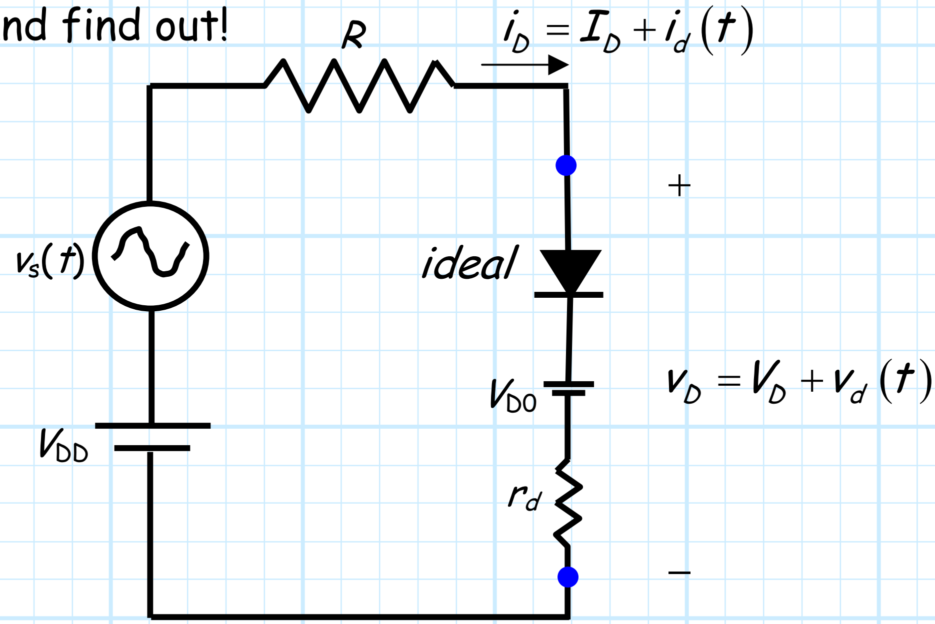
Now let's add an **AC** (e.g., small-signal) source (v_d) to the circuit:



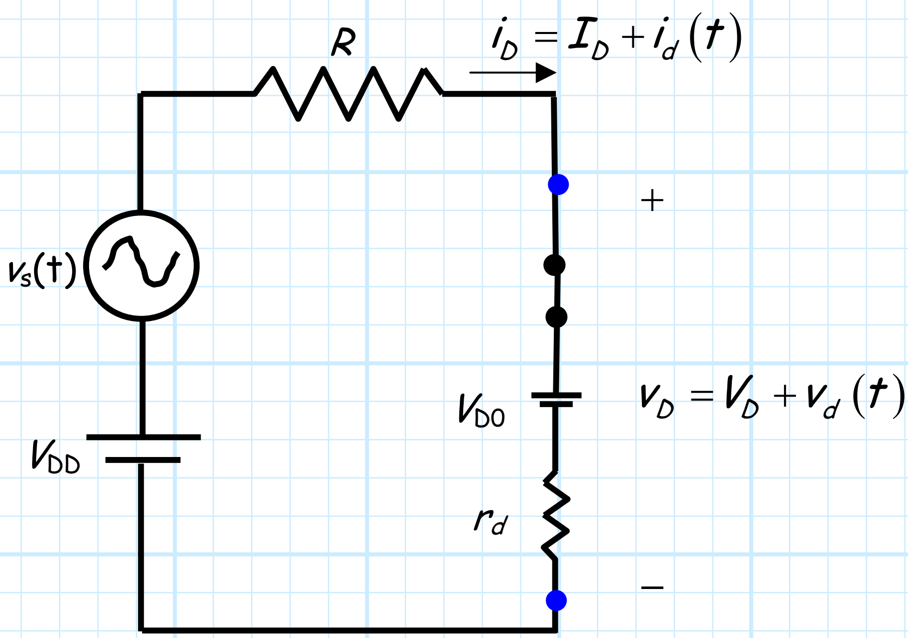
Note that this results in an **additional AC** (small-signal) **component** for the junction diode current and voltage.

Q: *What **are** the DC and small-signal components of the **diode** current and voltage, and how are they **related** to the DC (V_{DD}) and small-signal (v_s) voltage sources?*

A: Let's replace the junction diode with a small-signal PWL model and find out!



If the DC voltage source is sufficiently large (e.g.,, $V_{DD} \gg V_{D0}$), we will find that the ideal diode is **forward biased** ($v_D^i = 0$):



Now, let's apply **KVL** and analyze the circuit!

First, we'll consider the case where the **small-signal voltage source is zero** ($v_s(t) = 0$). In this case, the remaining **DC** sources (V_{DD} and V_{D0}) produce a DC voltage and current (V_D and I_D).

These DC values are related from KVL as:

$$V_{DD} = I_D(R + r_d) + V_{D0}$$

We call this the **DC circuit equation**.

Now let's "**turn on**" the small-signal source, so that $v_s(t) \neq 0$. Now we have, in **addition** to the DC currents and voltages, **small-signal components** i_d and v_d as well!

Again using **KVL**, we find that the DC and small-signal components are related as:

$$\begin{aligned} V_{DD} + v_s &= (I_D + i_d)R + V_{D0} + (I_D + i_d)r_d \\ &= (R + r_d)I_D + V_{D0} + (R + r_d)i_d \end{aligned}$$

Now, just for fun, let's **subtract** the **DC equation** from this KVL:

$$\begin{aligned} v_s + V_{DD} &= (R + r_d)I_D + V_{D0} + (R + r_d)i_d \\ -V_{DD} &= -(R + r_d)I_D - V_{D0} \end{aligned}$$

$$v_s = (R + r_d)i_d$$

The resulting equation:

$$v_s(t) = (R + r_d)\, i_d(t)$$

is known as the AC, or **small-signal circuit equation**.

Thus, the **total** KVL can be divided into two parts, the DC equation and the small-signal equation, i.e.:

$$V_{DD} + v_s = (R + r_d) I_D + V_{D0} + (R + r_d)\, i_d$$

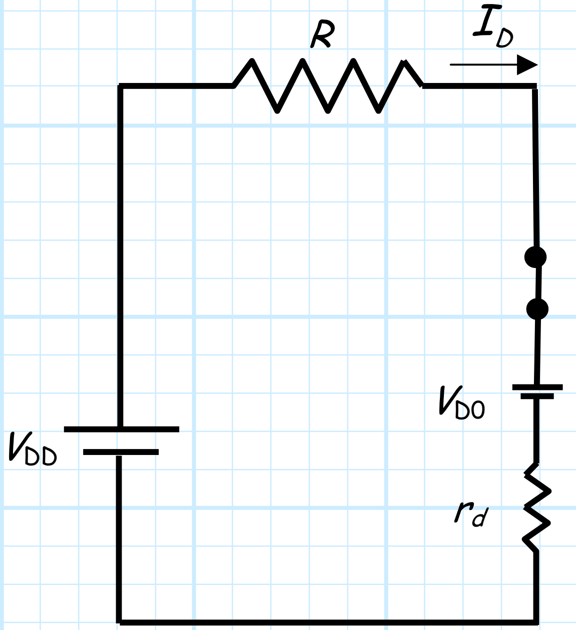
were the **DC equation** is:

$$V_{DD} = (R + r_d) I_D + V_{D0}$$

and the **small-signal equation** is:

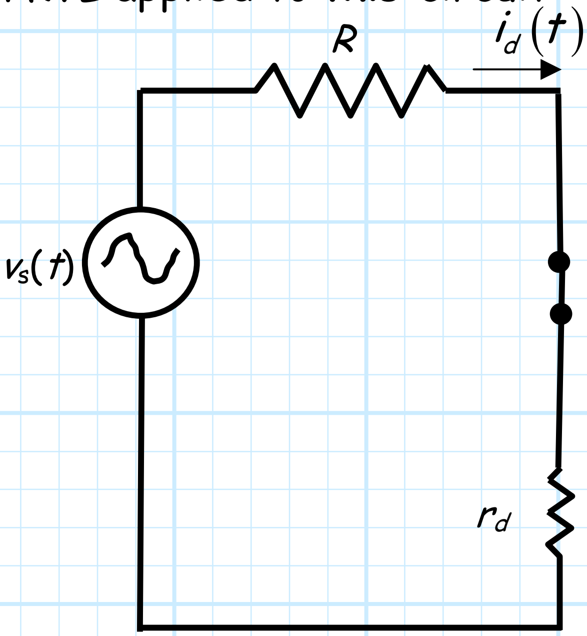
$$v_s = (R + r_d)\, i_d$$

Now, it is **very important** that you note this interesting result. The DC equation can be **directly derived** from KVL applied to **this** circuit:



$$V_{DD} = (R + r_d) I_D + V_{D0}$$

Likewise, the small-signal equation can be **directly derived** from KVL applied to **this** circuit:



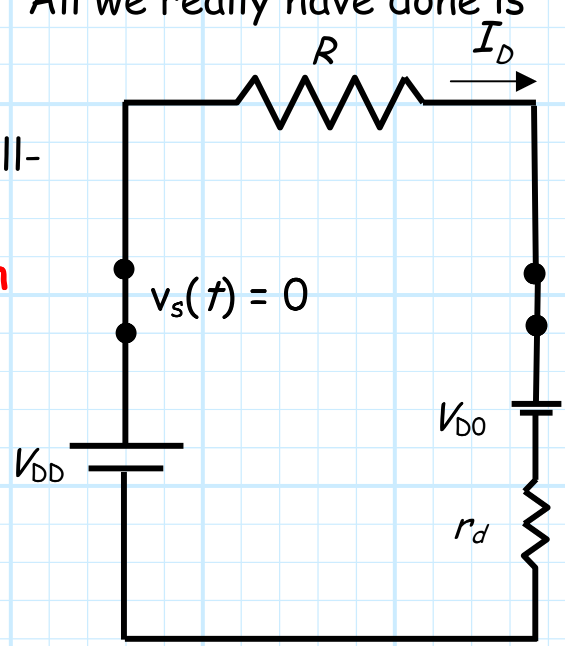
$$v_s(t) = (R + r_d)\, i_d(t)$$

Just as we can separate the total circuit KVL equation into DC and small-signal equations, we can **separate** the total **circuit** into DC and small-signal **circuits**!

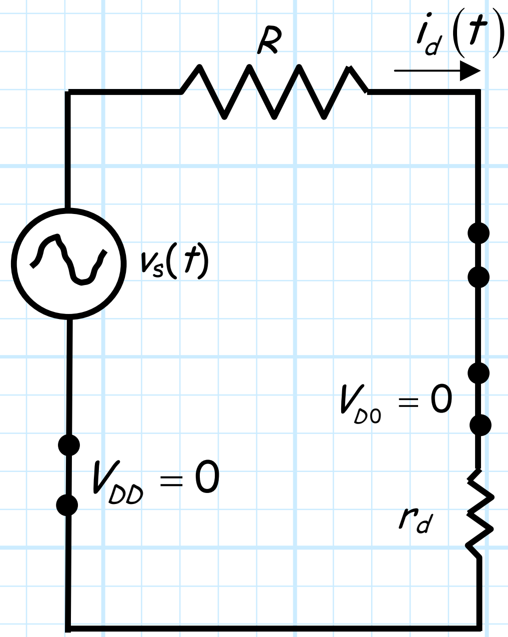
Look **closely** at the two circuits. All we really have done is apply **superposition!** I.E.:

1. We turned **off** the small-signal source and then determined the **DC solution** (i.e., the DC equation):

$$V_{DD} = (R + r_d) I_D + V_{D0}$$



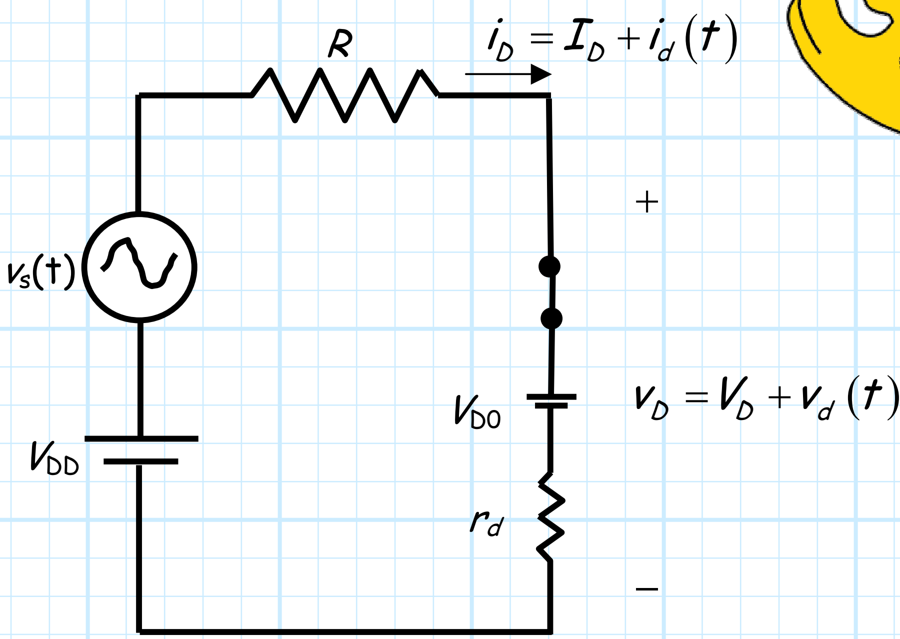
2. We then turned **off** the DC sources and determined the **small-signal solution** (i.e., the small-signal equation):



$$v_s(t) = (R + r_d)\, i_d(t)$$

Q: *Hold on dude! Earlier in the course you said that diodes are **non-linear** devices, meaning that superposition **cannot** be applied!?!*

A: True! But look at the circuit we are analyzing—there are **no diodes** in this circuit!

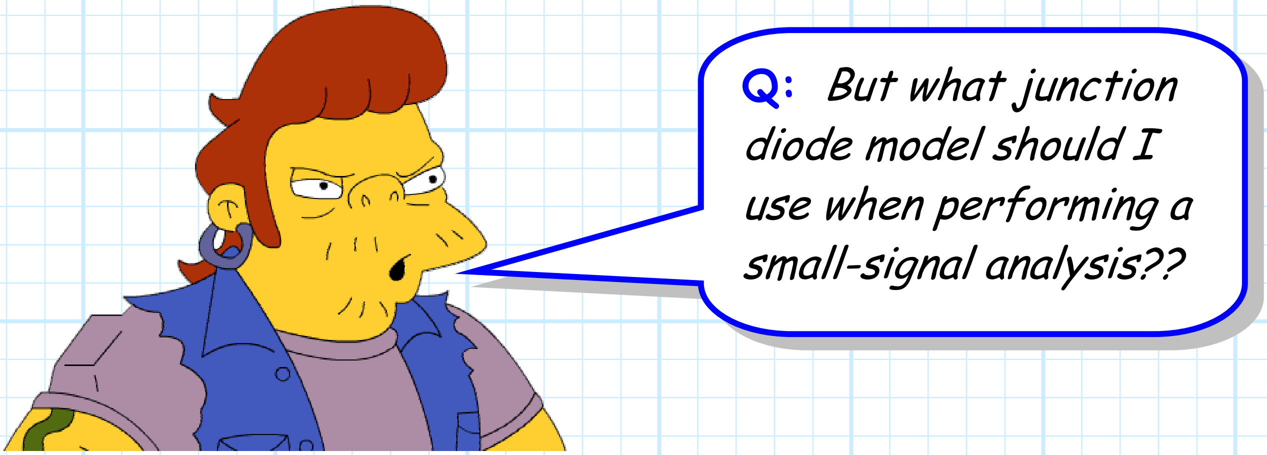


* Recall the (assumed) forward biased ideal diode was replaced with a **short circuit**—and a short circuit is a linear device!

* Thus, applying superposition to this circuit is a valid analysis technique, provided that **ideal** diode **remains forward biased** for all time t (i.e., $i_D(t) > 0$ for all time t).

* If the DC source is sufficiently large to place the ideal diode "firmly" into forward bias (i.e., $I_D \gg 0$), then the addition of a small AC source (i.e., the small signal source) will typically **not** change the ideal bias state (i.e., $I_D + i_d(t) > 0$ for all t).

Thus, we can perform a **small-signal analysis** of a junction diode circuit (once a junction diode **model** is applied) by applying **superposition**—turn **off** the DC sources and analyze the resulting **small-signal circuit!**



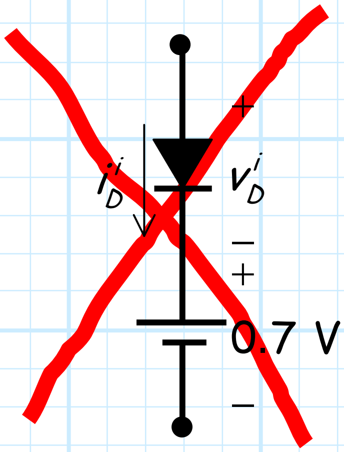
A: We can theoretically use **any** valid diode model (e.g., CVD, PWL) in a small-signal analysis. However, when we consider the type of small signal problem that we **typically** encounter, we find that **one model** stands out as **most** appropriate.

Consider the **total** diode current and **total** diode voltage when **both** DC and small-signal components are present:

$$i_D(t) = I_D + i_d(t)$$

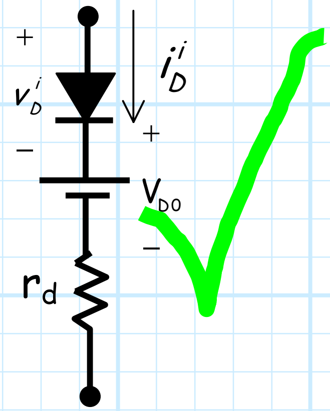
$$v_D(t) = V_D + v_d(t)$$

First of all, we can assume that the small-signal current i_d and small-signal voltage v_d is indeed—**small**. As such, we typically need some **precision** in our diode model if we are in search of **accurate** small-signal estimates.

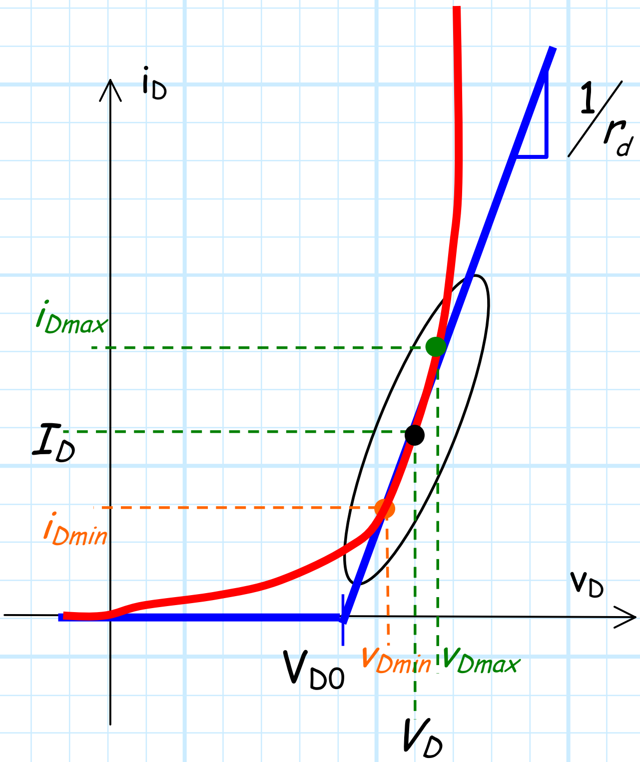


For example, the **CVD** model would **always** provide an estimate of the small-signal diode voltage of $v_d(t)=0$ (i.e., for CVD $v_D(t)$ =0.7 V always, thus V_D=0.7 V and v_d=0 **always**!)—this is **not** precise enough!

Thus we might conclude that a **PWL model** is our best bet. The problem then becomes how to **construct** this model (i.e., **what values** of r_D and V_{D0} should we use??).

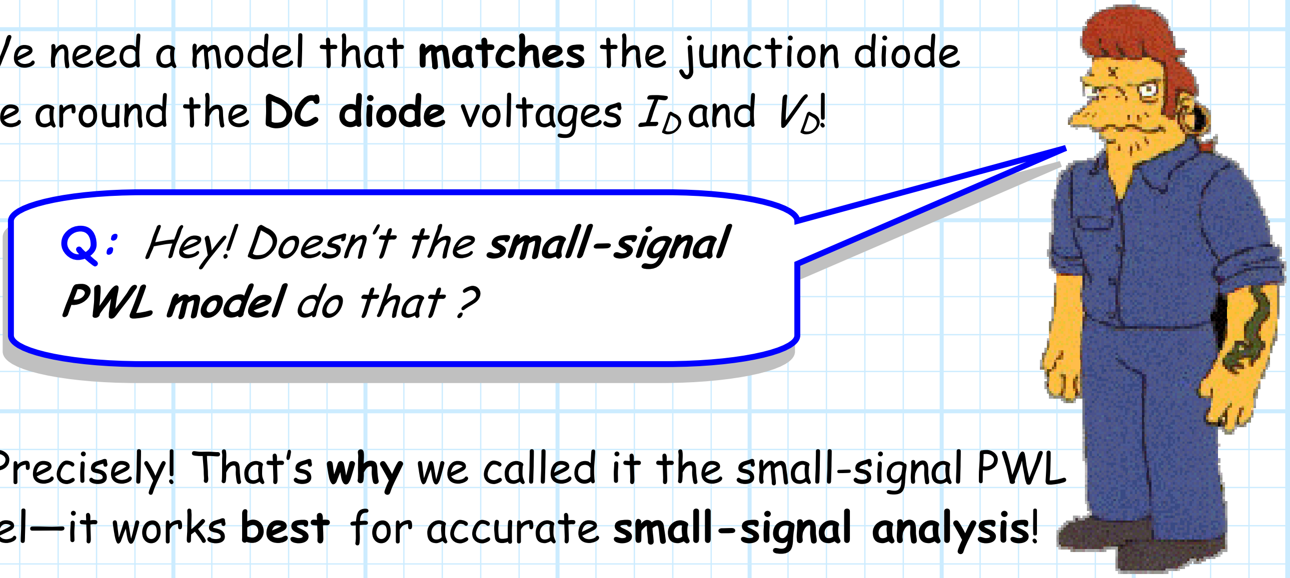


First, we note that since if the small-signal diode currents and voltages are **small**, the **largest total** diode current and **total** diode voltage ($i_D(t)$ and $v_D(t)$) will **never** be much larger than the **DC** diode current and voltage I_D and V_D.



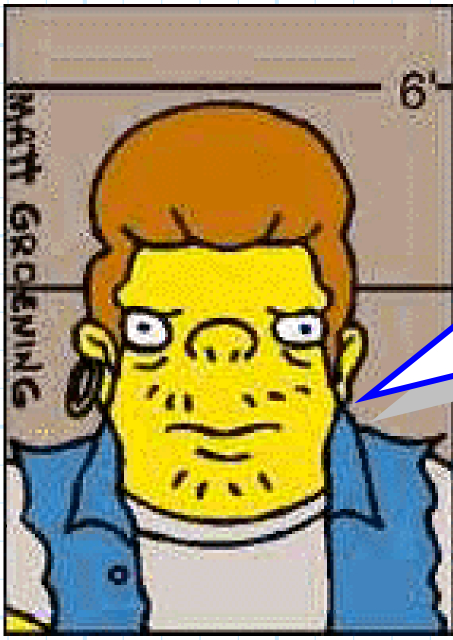
Likewise, the **smallest total** diode voltage and **total** diode current will **never** be much smaller than the **DC** diode current and voltage I_D and V_D.

→ We need a model that **matches** the junction diode curve around the **DC diode** voltages I_D and V_D!



A: Precisely! That's **why** we called it the small-signal PWL model—it works **best** for accurate **small-signal analysis**!

The DC diode current I_D and voltage V_D is the "**bias point**" that we spoke of when explaining the small-signal PWL model. Recall that **once** we determine these DC bias values, we can **immediately** find the model values of V_{D0} and r_D !



Q: *But dude, how can I determine the DC "bias" values I_D and V_D if I do not **first** know the parameters (V_{D0} and r_D) of my PWL junction diode **model**?*

A: Easy! We simply perform a **DC analysis** with the **DC circuit** to find I_D and V_D. The "trick" is that we perform the DC analysis using the **CVD model**—and we **know** the model parameters of the CVD model!

1. Replace junction diodes with CVD model.

2. Turn "off" ss sources.

3. Perform DC analysis to find DC bias.

4. Calculate ss PWL model values.

5. Replace junction diodes with ss PWL model.

6. Turn off DC sources (including V_{D0})!

7. Perform ss analysis.